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EXAMINER	
ROSENBERGER, FREDERICK F	
ART UNIT	**PAPER NUMBER**
2884	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/502,465	NASSIOPOULOU ET AL.	
	Examiner	Art Unit	
	Frederick F. Rosenberger	2884	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's reply, filed 21 November 2005, has been received and entered. Accordingly, changes have been made to the specification. Claims 1-10 have been cancelled. Claims 11-30 have been added. Thus, claims 11-30 are currently pending in this application.

2. The drawings were received on 21 November 2005. These drawings are acceptable.

Claim Objections

3. Claims 14 and 27-30 are objected to because of the following informalities:

In claim 14, lines 12-14, the recitation of "the depositing and patterning of aluminum to form the metal pads and interconnects optionally simultaneously forming the second thermocouple, if aluminum, to form a sensor" is awkward and confusing. Said recitation may be clearer by rephrasing to distinguish that the step of forming the metal pads and interconnects may optionally occur simultaneously with the step of forming the second thermocouple.

In claim 27, lines 2-3, the recitation of "the crystalline silicon layer" lacks proper antecedent basis in claim 26, which only defines a bulk crystalline layer. Subsequent recitations of "crystalline silicon" or "bulk

crystalline silicon" in claims 28-30 also lack antecedent basis in claim 26 on the same grounds.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 26 is rejected under 35 U.S.C. 102(b) as being anticipated by Angelucci et al. (Journal paper entitled "Permeated Porous Silicon for Hydrocarbon Sensor Fabrication").

Angelucci et al. disclose a processed silicon article comprising a bulk crystalline silicon layer, in the form of a silicon substrate (Figure 1), with a cavity disposed therein in the vicinity of a first outer surface of the bulk crystalline layer (i.e. the top surface of the device in Figure 1), and a localized porous silicon membrane disposed over the cavity, wherein the outer surface of the porous silicon membrane is aligned with the first outer surface of the bulk crystalline layer.

6. Claims 11, 12, and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Lammel et al. (Journal paper entitled "Free-Standing, Mobile 3D Porous Silicon Microstructures").

With regards to claim 11, Lammel et al. disclose a method of processing silicon comprising the steps of locally forming porous silicon in a first side of a crystalline silicon substrate by electrochemical dissolution at a current density sufficiently low to avoid electropolishing (page 357, column 2, section 2.3; Figure 2) and then increasing the current density to form a cavity and a porous silicon membrane with the cavity disposed under the porous silicon membrane (Figure 4).

With regards to claim 12, Lammel et al. further disclose a masking layer, in the form of either a metal layer or insulating mask, for the formation of the porous silicon membrane on a first side of the crystalline silicon substrate prior to the electrochemical dissolution (page 357, column 1, section 2.1; Figure 4).

With regards to claim 26, Lammel et al. disclose a processed silicon article comprising a bulk crystalline silicon layer, in the form of a silicon substrate (Figure 4), with a cavity disposed therein in the vicinity of a first outer surface of the bulk crystalline layer (i.e. the top surface of the device underneath the mask layer in Figure 4), and a localized porous silicon membrane disposed over the cavity, wherein the outer surface of the porous silicon membrane is aligned with the first outer surface of the bulk crystalline layer.

7. Claims 11-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Tjerkstra et al. (Journal paper entitled "Multi-Walled Microchannels: Free-Standing Porous Silicon Membranes for Use in μTAS").

With regards to claim 11, Tjerkstra et al. disclose a method of processing silicon comprising the steps of locally forming porous silicon in a first side of a crystalline silicon substrate by electrochemical dissolution at a current density sufficiently low to avoid electropolishing (page 495, section II, paragraphs 2 and 3) and then increasing the current density to form a cavity and a porous silicon membrane with the cavity disposed under the porous silicon membrane (Figure 1; page 496, section III(A), paragraph 4).

With regards to claim 12, Tjerkstra et al. further disclose a masking layer, in the form of a patterned silicon nitride layer, for the formation of the porous silicon membrane on a first side of the crystalline silicon substrate prior to the electrochemical dissolution (page 496, section III(A), paragraph 1).

With regards to claim 13, Tjersktra et al. further disclose the formation of an ohmic contact, in the form a 750-nm layer of aluminum, disposed on the back side of the crystalline silicon substrate prior to electrochemical dissolution (page 496, section III(A), paragraph 1).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to

be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 14, 15, and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaltsas et al. (Journal paper entitled "Novel C-mos Compatible Monolithic Silicon Gas Flow Sensor with Porous Silicon Thermal Isolation") in view of Lammel et al. (Journal paper entitled "Free-Standing, Mobile 3D Porous Silicon Microstructures").

With regards to claims 14, Kaltsas et al. disclose a method of processing silicon comprising:

Locally forming porous silicon in a first side of a crystalline silicon substrate by electrochemical dissolution to form a thermal isolation region of porous silicon (Region A in Figure 2, page 134);

Depositing a thin dielectric layer over the first layer of the silicon substrate, in the form of TEOS oxide for electrical isolation (page 134, column 2);

Depositing and patterning a polycrystalline silicon layer over the dielectric layer, in the form of a 500-nm polysilicon layer (page 134, column 2) and which partially overlaps the porous silicon region (Figure 2);

Doping the polycrystalline silicon with a p-type dopant, i.e. boron (page 135, column 1) to form a resistor heater and a first part of the thermopile, wherein a thermopile is a series of thermocouples;

And depositing and patterning aluminum in order to form the second part of the thermopile, and the metal pads/interconnects for the sensor (page 135, column 1);

Kaltsas et al. only provide the porous silicon as a thermal insulation layer from the bulk silicon. Kaltsas et al. do not address forming the porous silicon layer into porous silicon membrane through electropolishing. However, Kaltsas et al. do recognize the enhanced performance of thermal flow sensors associated with increased thermal isolation of the heater element from the bulk silicon using cavities (page 133, column 2).

It is well known in the art that the thermal conductivity of bulk silicon is much greater than that of porous silicon. As Kaltsas et al. point out, it is the use of this property that enables thermal isolation of the heating element from the bulk silicon without the formation of a cavity. It is further well known that the thermal conductivity of air is much lower than that of porous silicon. Thus, it

would stand to reason that the creation of an air gap between the heater and the bulk silicon would lead to even greater performance.

Lammel et al. teach a fabrication method for creating porous silicon membranes with cavities beneath them applicable to the invention of Kaltsas et al. Lammel et al. teach the steps of locally forming porous silicon in a first side of a crystalline silicon substrate by electrochemical dissolution at a current density sufficiently low to avoid electropolishing (page 357, column 2, section 2.3; Figure 2) and then increasing the current density to form a cavity and a porous silicon membrane with the cavity disposed under the porous silicon membrane (Figure 4).

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the method of Lammel et al. to create a cavity underneath a porous silicon membrane to further enhance the thermal isolation of the heating element for enhanced sensor performance since it is well known in the art that an air cavity would give increased thermal isolation compared to a layer of porous silicon.

With regards to claim 15, Kaltsas et al. disclose the formation of a thermopile, which is a series of thermocouples.

With regards to claim 27, Kaltsas et al. disclose a processed silicon article, in the form of a thermal gas flow sensor, comprising:

> A porous silicon thermal isolation region (Region A in Figure 2, page 134) formed in a bulk silicon crystalline layer, wherein the surface of the bulk silicon and porous silicon are coplanar;

A thin dielectric layer over the first layer of the silicon substrate, in the form of TEOS oxide for electrical isolation (page 134, column 2);

A patterned 500-nm polysilicon layer (page 134, column 2) partially overlapping the porous silicon region (Figure 2);

A first portion of the patterned polysilicon layer which is p-doped (page 135, column 1) forming a resistor heater (Figure 2)

A second portion of the patterned polysilicon layer, which is p-doped forming a first part of a thermopile, which is a series of thermocouples;

A second part of thermopile disposed on the dielectric layer, wherein said second part is patterned aluminum (page 135, column 1);

And pairs of aluminum metal pads and interconnects on the dielectric layer (page 135, column 1; Figure 2).

Kaltsas et al. only provide the porous silicon as a thermal insulation layer from the bulk silicon. Kaltsas et al. do not address forming the porous silicon layer into porous silicon membrane through electropolishing. However, Kaltsas et al. do recognize the enhanced performance of thermal flow sensors associated with increased thermal isolation of the heater element from the bulk silicon using cavities (page 133, column 2).

It is well known in the art that the thermal conductivity of bulk silicon is much greater than that of porous silicon. As Kaltsas et al. point out, it is the use of this property that enables thermal isolation of the heating element from the bulk silicon without the formation of a cavity. It is further well known that the

thermal conductivity of air is much lower than that of porous silicon. Thus, it would stand to reason that the creation of an air gap between the heater and the bulk silicon would lead to even greater performance.

Lammel et al. teach a fabrication method for creating porous silicon membranes with cavities beneath them applicable to the invention of Kaltsas et al. Lammel et al. teach the steps of locally forming porous silicon in a first side of a crystalline silicon substrate by electrochemical dissolution at a current density sufficiently low to avoid electropolishing (page 357, column 2, section 2.3; Figure 2) and then increasing the current density to form a cavity and a porous silicon membrane with the cavity disposed under the porous silicon membrane (Figure 4).

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the method of Lammel et al. to create a cavity underneath a porous silicon membrane to further enhance the thermal isolation of the heating element for enhanced sensor performance since it is well known in the art that an air cavity would give increased thermal isolation compared to a layer of porous silicon.

With regards to claim 28, Kaltsas et al. disclose that the hot contacts of the thermopiles are close to the polysilicon heater over the porous silicon region and the cold contacts are outside the porous silicon region and on the bulk silicon (Figure 1; page 134, column 1).

With regards to claim 29, Kaltsas et al. disclose that the interconnects and metal pads are disposed over the bulk silicon (Figures 1 and 2).

11. Claims 16-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaltsas et al. and Lammel et al., as applied to claim 15 above, and further in view of Sabate et al. (Conference paper entitled "Evaluation of Sensitive Materials for Integrated Thermal Flow Sensors").

With regards to claims 16 and 17, the combination of Kaltsas et al. and Lammel et al. disclose all the limitations of parent claim 15, as discussed above. However, neither Kaltsas et al. nor Lammel et al. specifically address the formation of a passivation layer or an insulating passivation layer.

However, it is well known in the art that passivation layers are often included, especially with gas or fluid sensors, so as to prevent corrosion of the sensor upon exposure to various chemicals. For example, Sabate et al. disclose that it is common to form a passivation layer of either silicon nitride of silicon dioxide on the sensor after formation of the heater/sensor elements so as to preserve the resistors from contamination and degradation (page 2682, column 2, section IV).

Thus, it would have been obvious for a person having ordinary skill in the art at the time the invention was made to provide a passivation layer of either silicon nitride or silicon dioxide on the thermal flow sensor so as to prevent contamination and degradation of the sensor elements, as taught by Sabate et al.

With regards to claim 18, Kaltsas et al. disclose that the hot contacts of the thermopiles are close to the polysilicon heater over the porous silicon region

and the cold contacts are outside the porous silicon region and on the bulk silicon (Figure 1; page 134, column 1).

With regards to claim 19, Kaltsas et al. disclose that the interconnects and metal pads are disposed over the bulk silicon (Figures 1 and 2).

With regards to claims 20 and 21, the combination of Kaltsas et al., Lammel et al., and Sabate et al. already address the inclusion of a passivation layer of silicon oxide or silicon nitride, as discussed above with regards to claims 16 and 17.

12. Claims 22, 25, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaltsas et al. and Lammel et al. in view of Hedrich et al. (Journal paper entitled "Structuring of Membrane Sensors Using Sacrificial Porous Silicon").

With regards to claims 22 and 25, Kaltsas et al. disclose a method of processing silicon to form a thermal flow sensor comprising:

Locally forming porous silicon in a first side of a crystalline silicon substrate by electrochemical dissolution to form a thermal isolation region of porous silicon (Region A in Figure 2, page 134);

Depositing a thin dielectric layer over the first layer of the silicon substrate, in the form of TEOS oxide for electrical isolation (page 134, column 2);

Depositing and patterning a polycrystalline silicon layer over the dielectric layer, in the form of a 500-nm polysilicon layer (page 134, column 2) and which partially overlaps the porous silicon region (Figure 2);

Doping the polycrystalline silicon with a p-type dopant, i.e. boron (page 135, column 1) to form a resistor heater and a first part of the thermopile, wherein a thermopile is a series of thermocouples;

And depositing and patterning aluminum in order to form the second part of the thermopile, and the metal pads/interconnects for the sensor (page 135, column 1);

Wherein a first thermopile is formed on one side of the heater and a second thermopile is formed on the opposite side of the heater (Figure 1; page 133, column 2)

Kaltsas et al. only provide the porous silicon as a thermal insulation layer from the bulk silicon. Kaltsas et al. do not address forming the porous silicon layer into porous silicon membrane through electropolishing. However, Kaltsas et al. do recognize the enhanced performance of thermal flow sensors associated with increased thermal isolation of the heater element from the bulk silicon using cavities (page 133, column 2).

It is well known in the art that the thermal conductivity of bulk silicon is much greater than that of porous silicon. As Kaltsas et al. point out, it is the use of this property that enables thermal isolation of the heating element from the bulk silicon without the formation of a cavity. It is further well known that the thermal conductivity of air is much lower than that of porous silicon. Thus, it

would stand to reason that the creation of an air gap between the heater and the bulk silicon would lead to even greater performance.

Lammel et al. teach a fabrication method for creating porous silicon membranes with cavities beneath them applicable to the invention of Kaltsas et al. Lammel et al. teach the steps of locally forming porous silicon in a first side of a crystalline silicon substrate by electrochemical dissolution at a current density sufficiently low to avoid electropolishing (page 357, column 2, section 2.3; Figure 2) and then increasing the current density to form a cavity and a porous silicon membrane with the cavity disposed under the porous silicon membrane (Figure 4).

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the method of Lammel et al. to create a cavity underneath a porous silicon membrane to further enhance the thermal isolation of the heating element for enhanced sensor performance since it is well known in the art that an air cavity would give increased thermal isolation compared to a layer of porous silicon.

Kaltsas et al. are further silent with regards opening an inlet and outlet to the cavity through the silicon dioxide layer, thus forming a channel from the cavity underneath the porous silicon membrane.

The creation of microfluidic channels with associated sensors is not new in the art. Further, the use of an etched cavity underneath a membrane as a microfluidic channel is well known in the art. For example, Hedrich et al. use a silicon nitride membrane suspended over a cavity in a thermal flow sensor

(Figure 1). In such a configuration, the cavity between the substrate and the membrane can be used as a cavity for thermal isolation or as a channel, as indicated.

The fabrication methods associated with opening an inlet and/or outlet in a silicon dioxide layer and the porous silicon layer are well known in the art. For example, silicon dioxide can be easily etched using photolithography and conventional hydrofluoric acid etching techniques. Similarly, both Lammel et al. (page 355, column 1) and Kaltsas et al. (page 133, column 2) address conventional techniques for etching porous silicon and silicon respectively.

Thus, it would have been obvious for a person having ordinary skill in the art at the time the invention was made to use the cavity underneath the porous silicon membrane as a channel, as taught by Hedrich et al. and provide the necessary inlet and outlet connections to use it as such, so as to provide an integrated sensor and sample flow containment system, without the addition of additional external structure for directing the sample flow across the sensor elements.

The microfluidic nature of the device would be inherent by virtue of the micromachining process and corresponding microstructure of the channel.

With regards to claim 30, Kaltsas et al. disclose a processed silicon article, in the form of a thermal gas flow sensor, comprising:

> A porous silicon thermal isolation region (Region A in Figure 2, page 134) formed in a bulk silicon crystalline layer, wherein the surface of the bulk silicon and porous silicon are coplanar;

A thin dielectric layer over the first layer of the silicon substrate, in the form of TEOS oxide for electrical isolation (page 134, column 2);

A patterned 500-nm polysilicon layer (page 134, column 2) partially overlapping the porous silicon region (Figure 2);

A first portion of the patterned polysilicon layer which is p-doped (page 135, column 1) forming a resistor heater (Figure 2)

A second portion of the patterned polysilicon layer, which is p-doped forming a first part of a thermopile, which is a series of thermocouples;

A second part of thermopile disposed on the dielectric layer, wherein said second part is patterned aluminum (page 135, column 1);

And pairs of aluminum metal pads and interconnects on the dielectric layer (page 135, column 1; Figure 2).

Kaltsas et al. only provide the porous silicon as a thermal insulation layer from the bulk silicon. Kaltsas et al. do not address forming the porous silicon layer into porous silicon membrane through electropolishing. However, Kaltsas et al. do recognize the enhanced performance of thermal flow sensors associated with increased thermal isolation of the heater element from the bulk silicon using cavities (page 133, column 2).

It is well known in the art that the thermal conductivity of bulk silicon is much greater than that of porous silicon. As Kaltsas et al. point out, it is the use of this property that enables thermal isolation of the heating element from the bulk silicon without the formation of a cavity. It is further well known that the

thermal conductivity of air is much lower than that of porous silicon. Thus, it would stand to reason that the creation of an air gap between the heater and the bulk silicon would lead to even greater performance.

Lammel et al. teach a fabrication method for creating porous silicon membranes with cavities beneath them applicable to the invention of Kaltsas et al. Lammel et al. teach the steps of locally forming porous silicon in a first side of a crystalline silicon substrate by electrochemical dissolution at a current density sufficiently low to avoid electropolishing (page 357, column 2, section 2.3; Figure 2) and then increasing the current density to form a cavity and a porous silicon membrane with the cavity disposed under the porous silicon membrane (Figure 4).

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the method of Lammel et al. to create a cavity underneath a porous silicon membrane to further enhance the thermal isolation of the heating element for enhanced sensor performance since it is well known in the art that an air cavity would give increased thermal isolation compared to a layer of porous silicon.

Kaltsas et al. are further silent with regards an inlet and outlet to the cavity through the silicon dioxide layer, thus forming a channel from the cavity underneath the porous silicon membrane.

The creation of microfluidic channels with associated sensors is not new in the art. Further, the use of an etched cavity underneath a membrane as a microfluidic channel is well known in the art. For example, Hedrich et al. use a

silicon nitride membrane suspended over a cavity in a thermal flow sensor (Figure 1). In such a configuration, the cavity between the substrate and the membrane can be used as a cavity for thermal isolation or as a channel, as indicated.

Thus, it would have been obvious for a person having ordinary skill in the art at the time the invention was made to use the cavity underneath the porous silicon membrane as a channel, as taught by Hedrich et al. and provide the necessary inlet and outlet connections to use it as such, so as to provide an integrated sensor and sample flow containment system, without the addition of additional external structures for directing the sample flow across the sensor elements.

13. Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaltsas et al., Lammel et al., and Hedrich et al., as applied to claim 22 above, and further in view of Sabate et al. (Conference paper entitled "Evaluation of Sensitive Materials for Integrated Thermal Flow Sensors").

With regards to claims 23 and 24, the combination of Kaltsas et al., Lammel et al., and Hedrich et al. disclose all the limitations of parent claim 22, as discussed above. However, the cited references fail to disclose the forming of a passivation layer on top of the sensor.

However, it is well known in the art that passivation layers are often included, especially with gas or fluid sensors, so as to prevent corrosion of the sensor upon exposure to various chemicals. For example, Sabate et al. disclose

that it is common to form a passivation layer of either silicon nitride of silicon dioxide on the sensor after formation of the heater/sensor elements so as to preserve the resistors from contamination and degradation (page 2682, column 2, section IV).

Thus, it would have been obvious for a person having ordinary skill in the art at the time the invention was made to provide a passivation layer of either silicon nitride or silicon dioxide on the thermal flow sensor so as to prevent contamination and degradation of the sensor elements, as taught by Sabate et al.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Lee et al. (US Patent # 5,565,084) teach the use of a metal layer on the backside of a silicon wafer in a single sided electrochemical cell for the formation of porous silicon (Figure 2).

Benzei et al. (US Patent # 6,803,637) teach the formation of microfluidic channels underneath a porous silicon membrane as well as inlets and outlets to the buried channels (e.g. Figures 5 and 6).

Tu (US Patent # 6,139,758) teach the use of passivation layers in thermopile gas flowmeters was well known. Tu also teach that the presently claimed layout of the heater and thermocouples was well known (Figure 1; column 1, lines 26-37).

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Frederick F. Rosenberger whose telephone number is 571-272-6107. The examiner can normally be reached on Monday-Friday 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Porta can be reached on 571-272-2444. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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